IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sanzo	**Examiner: Ton, My Trang**
Serial No.: 10/748,861	Group Art Unit: 2816
Filed: December 30, 2003	Confirm. No. 3695
For: FREQUENCY SELECTION OF SWITCH MODE POWER CONVERTERS VIA SOFTSTART VOLTAGE LEVEL	Docket No. TI-36644

DECLARATION OF CHRISTOPHER J. SANZO
Pursuant to 37 C.F.R. § 1.132

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

I, Christopher J. Sanzo, hereby declare that:

1. Texas Instruments Incorporated is the assignee of the above-identified patent application.
2. I have reviewed the above-identified patent application, including the claims. I am the inventor of the invention claimed in the above-identified patent application.
3. As a Texas Instruments Incorporated employee, I was assigned the responsibility of developing notebook power controllers.
4. The invention claimed in the above-identified patent application was embodied in the TPS51020 device.
5. I have reviewed the Texas Instruments publication cited by the Patent Examiner in the parent application. The Texas Instruments publication is entitled "DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER", dated July 2003 (Revised November 2003). A copy of the Texas Instruments publication is attached hereto as Exhibit A. This publication is a data sheet for the TPS51020 device.

6. The Texas Instruments publication was published on my behalf, I was the primary author of the publication, and the subject matter disclosed in the publication related to my invention is attributable to me.

I, Christopher J. Sanzo, hereby declare that all statements herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made knowing that willful false statements and the like are punishable by fine or imprisonment, or both under § 1001 of Title 18 of United States Code, and such willful or false statements may jeopardize the validity of the above-identified application or any patent issuing therefrom.

Respectfully submitted,

Date: 8/3/2006

Christopher J. Sanzo

Exhibit A

TEXAS INSTRUMENTS

SLUS564A – JULY 2003 – REVISED NOVEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

FEATURES

- Wide Input Voltage Range: 4.5-V to 28-V
- Selectable Dual and DDR Modes
- Selectable Fixed Frequency Voltage Mode
- Integrated Selectable Output Discharge
- Advanced Power Good Logic Monitors both Channels
- Selectable Autoskip Mode
- Integrated Boot Strap Diodes
- 180° Phase Shift Between Channels
- Integrated 5-V, 60-mA Regulator
- Input Feedforward Control
- 1% Internal 0.85-V Reference
- $R_{DS(on)}$ Overcurrent Detection (4200 ppm/°C)
- Integrated OVP, UVP and Power Good Timers
- 30-pin TSSOP Package

APPLICATIONS

- Notebook Computers System Bus and I/O
- DDR I or DDR II Termination

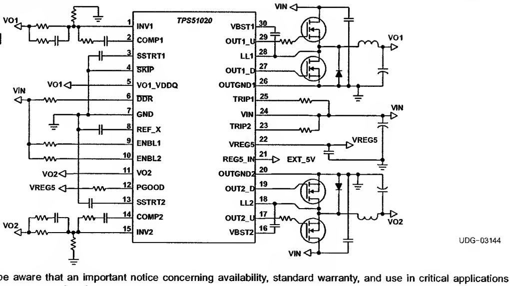
DESCRIPTION

The TPS51020 is a multi-function dual-synchronous step-down controller for notebook system power. The part is specifically designed for high performance, high efficiency applications where the loss associated with a current sense resistor is unacceptable. The TPS51020 utilizes feed forward voltage mode control to attain high efficiency without sacrificing line response. Efficiency at light load conditions can be maintained high as well by incorporating autoskip operation. A selectable, Suspend to RAM (STR) supported, DDR option provides a one chip solution for all switching applications from 5-V/3.3-V supply to a complete DDR termination solution.

ORDERING INFORMATION

TA	PLASTIC TSSOP (DBT)
–40°C to 85°C	TPS51020DBT
	TPS51020DBTR (T&R)

SIMPLIFIED APPLICATION DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted. All voltage values are with respect to the network ground terminal unless otherwise noted. (1)

		TPS51020	UNIT
Input voltage range	VBST1, VBST2	–0.3 to 35	V
	VBST1, VBST2 (with respect to LL)	-0.3 to 7	
	VIN, TRIP1, TRIP2, ENBL1, ENBL2, $\overline{\text{DDR}}$	-0.3 to 30	
	$\overline{\text{SKIP}}$, INV1, INV2	-0.3 to 7	
Ouput voltage range	OUT1_U, OUT2_U	–1 to 35	
	OUT1_U, OUT2_U (with respect to LL)	-0.3 to 7	
	LL1, LL2	–1 to 30	
	REF_X	–0.3 to 15	
	PGOOD, VO1_VDDQ, VO2, OUT1_D, OUT2_D, COMP1, COMP2, VREG5, SSTRT1, SSTRT2	-0.3 to 7	
	OUTGND1, OUTGND2	-0.3 to 0.3	
Output current range	VREG5	70	mA
	REF_X	7	
Operating free-air temperature range, T_A		–40 to 85	°C
Storage temperature range, T_{stg}		-55 to 150	
Junction temperature range, T_J		-40 to 125	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

RECOMMENDED OPERATING CONDITIONS

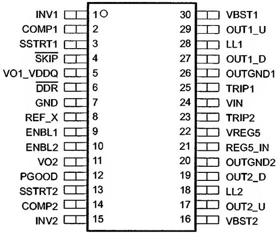
		MIN	TYP	MAX	UNIT
Supply voltage, VIN		4.5		28	V
Supply voltage, VBST1, VBST2		4.5		33	
I/O Voltage	ENBL1, ENBL2, $\overline{\text{DDR}}$, TRIP1, TRIP2	–0.1		28	
	OUT1_U, OUT2_U	–0.8		33	
	OUT1_U, OUT2_U (with respect to LL)	–0.1		5.5	
	LL1, LL2	–0.8		28	
	REF_X	–0.1		12	
	SSTRT1, SSTRT2, COMP1, COMP2	–0.1		5.5	
	$\overline{\text{SKIP}}$, INV1, INV2	–0.1		5.5	
	PGOOD VO1_VDDQ, VO2	–0.1		5.5	
	OUT1_D, OUT2_D, VREG5	–0.1		5.5	
Source current	VREG5			60	mA
	REF_X			5	
Operating free-air temperature, T_A		–40		85	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
30-pin DBT	874 mW	7.0 mW/°C	454 mW

TSSOP (0.5 mm)
DBT PACKAGE
(TOP VIEW)



ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, 4.5 V < V_{IN} < 20 V, C_{VIN} = 0.1 µF, C_{VREG5} = 2.2 µF, C_{REF_X} = 0.01 µF, PGOOD = 0.2 V, ENBLx = $\overline{\text{DDR}}$ = VIN, INVx = COMPx, RSSTRTx = OPEN, TRIP1 = TRIP2 = VIN, LLx = GND, VBSTx = LLx+5, $C_{(OUTx\_U,\ OUTx\_D)}$=1 nF, REG5_IN = 0V, GND = OUTGNDx = 0 V, VO1_VDDQ = VO2 = 0 V (unless otherwise stated)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENTS							
I_{VIN}	V_{IN} supply current	REG5V_IN = OPEN, OSC = OFF	TRIPx = VIN,		1.4	2.2	mA
$I_{VIN(STBY)}$	V_{IN} standby current	ENBLx = 0 V, REG5V_IN = OPEN,	$\overline{\text{DDR}}$ = VIN, OSC = OFF		350	550	µA
$I_{VIN(SHDN)}$	V_{IN} shutdown current	ENBLx = $\overline{\text{DDR}}$ = 0 V, REG5V_IN = OPEN			0.05	1.00	
$I_{VIN(REG5)}$	V_{IN} supply current, REG5_IN as 5-V input current	REG5V_IN = 5 V,	OSC = OFF		200	500	
I_{REG5}	REG5_IN input supply current	REG5V_IN = 5 V,	OSC = OFF		1.0	1.7	mA
I_{VBSTx}	VBST supply current	ENBLx = $\overline{\text{DDR}}$ = VIN			0.05	1.00	µA
I_{VBSTx}	VBST shutdown current	ENBLx = $\overline{\text{DDR}}$ = 0 V			0.05	1.00	
VREG5 INTERNAL REGULATOR							
V_{VREG5}	VREG5 voltage	I_{OUT} = 0 A		4.8	5.0	5.2	V
V_{LD5}	Load regulation	0 mA ≤ I_{OUT} ≤ 50 mA,	V_{IN} = 12 V		0.6%	2.5%	
V_{LN5}	Line regulation	I_{OUT} = 20 mA,	7 V≤V_{IN} ≤ 28 V		0.4%	2.0%	
V_{THL}	UVLO threshold voltage	High to low		3.45	3.65	3.85	V
$V_{HYS(UV)}$	UVLO hysteresis			100	200	300	mV
$V_{TH(SW)}$	Switchover voltage	REG_IN voltage		4.2	4.5	4.8	V
$V_{HYS(SW)}$	Switchover hysteresis			50		250	mV

ELECTRICAL CHARACTERISTICS (continued)

T_A = −40°C to 85°C, 4.5 V < V_{IN} < 20 V, C_{VIN} = 0.1 µF, C_{VREG5} = 2.2 µF, C_{REF_X} = 0.01 µF, PGOOD = 0.2 V, ENBLx = $\overline{DDR}$ = VIN, INVx = COMPx, RSSTRTx = OPEN, TRIP1 = TRIP2 = VIN, LLx = GND, VBSTx = LLx+5, $C_{(OUTx\_U,\ OUTx\_D)}$=1 nF, REG5_IN = 0V, GND = OUTGNDx = 0 V, VO1_VDDQ = VO2 = 0 V (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REF_X REFERENCE VOLTAGE						
V_{REF10}	10-V reference voltage	V_{IN} = 14 V, I_{OUT} = 0 A	8.5	10.0	11.0	V
V_{LD10}	Load regulation	0 mA ≤ I_{OUT} ≤ 2 mA, V_{IN} = 18 V		-12%	-20%	
V_{LN10}	Line regulation	I_{OUT} = 100 µA, 14 V≤V_{IN} ≤28 V			5%	
V_{REFVTT}	VTT reference voltage	$\overline{DDR}$ = 0 V wrt VO1_VDDQ input divided by 2 V_{VO1} = 2.5 V			1.5%	
V_{REFVTT}	VTT reference load regulation	0 mA ≤ I_O ≤ 3 mA			0.75%	
POWERGOOD COMPARATORS						
$V_{THDUAL(PG)}$	PGOOD threshold (dual mode)	Undervoltage PGOOD	765	786	808	mV
		Overvoltage PGOOD	892	914	935	
$V_{THDDR(PG)}$	PGOOD threshold (DDR)	Undervoltage PGOOD, VO1_VDDQ = 2.5 V	1.12	1.14	1.16	V
		Overvoltage PGOOD, VO1_VDDQ = 2.5 V	1.28	1.30	1.32	
$T_{PG(del)}$	PGOOD delay time	Delay time from SSTRTx > 1.5 V to PGOOD going high, INVx > (1-%) × 0.85 = V_{TH}		2048		clks
DIGITAL CONTROL INPUTS						
V_{IH}	High-level input voltage, logic	$\overline{DDR}$, ENBL1, ENBL2, $\overline{SKIP}$	2.2			V
V_{IL}	Low-level input voltage, logic	$\overline{DDR}$, ENBL1, ENBL2, $\overline{SKIP}$			0.3	
I_{INLEAK}	Logic input leakage current	$\overline{DDR}$, ENBL1, ENBL2, $\overline{SKIP}$= 5 V			|1.0|	µA
VO1_VDDQ and VO2						
R_{VOUT}	VOx sink impedance	V_{VOUTx} = 0.5 V, fault engaged		6	10	Ω
V_{VOUTOK}	VOx low restart voltage	Fault condition removed, restart	0.30	0.35	0.40	V
$V_{VO2LEAK}$	VOx input leakage current	$\overline{DDR}$= VIN, VOx = 5 V			|1.0|	µA
R_{VOUT}	VO1_VDDQ input impedance	$\overline{DDR}$= 0		1.5		MΩ
UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
$V_{OVPDUAL}$	OVP trip output threshold (dual)	Sensed at INVx	935	952	969	mV
V_{OVPDDR}	OVP trip output threshold (DDR)	VO1_VDDQ = 2.5 V	1.31	1.35	1.39	V
$T_{OVP(del)}$	OVP propagation delay time(1)			20		µs
$V_{UVPDUAL}$	UVP trip output threshold (dual)	Sensed at INVx	510	553	595	mV
V_{UVPDDR}	UVP trip output threshold (DDR)	VO1_VDDQ = 2.5 V	750	813	875	
$T_{UVP(del)}$	UVP propagation delay time			4096		clks
OVERCURRENT and INPUT VOLTAGE UVLO PROTECTION						
$I_{TRIPSNK}$	TRIPx sink current	V_{TRIPx} = V_{IN} − 100 mV, T_A = 25°C	11.0	12.5	14.0	µA
$I_{TRIPSRC}$	TRIPx source current	V_{TRIPx} = 100 mV, T_A = 25°C	10	12.5	15.0	
TC_{ITRIP}	TRIP current temperature coeficient(1)	T_A = 25°C		4200		ppm/°C
V_{OCPHI}	High-level OCP comparator offset voltage(1)			0	|3.0|	mV
V_{OCPLO}	Low-level OCP comparator offset voltage(1)			0	|5.0|	
$V_{VINUVLO}$	VIN UVLO trip threshold	REF5V_IN = 4.8 V	3.7	3.9	4.1	V
V_{VINHYS}	VIN UVLO trip hysteresis		100	200	300	mV

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, 4.5 V < V_{IN} < 20 V, C_{VIN} = 0.1 µF, C_{VREG5} = 2.2 µF, C_{REF_X} = 0.01 µF, PGOOD = 0.2 V, ENBLx = $\overline{DDR}$ = VIN, INVx = COMPx, RSSTRTx = OPEN, TRIP1 = TRIP2 = VIN, LLx = GND, VBSTx = LLx+5, $C_{(OUTx\_U,\ OUTx\_D)}$=1 nF, REG5_IN = 0V, GND = OUTGNDx = 0 V, VO1_VDDQ = VO2 = 0 V (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
0.85-V REFERENCE CONTROL LOOP						
V_{REFCH1}	Error amplifier reference, channel 1 initial accuracy	Measure COMP1, COMP1= INV1, T_A = 25°C	0.84	0.85	0.86	V
V_{REFTC1}	Error amplifier reference, channel 1 change with accuracy			0.5%		
V_{REFLN1}	Error amplifier reference, channel 1 change with line			0.1%		
V_{CHMM}	Channel 2 to channel 1 voltage mismatch			0	|5.0|	mV
CONTROL LOOP: SKIP HYSTERSTIC COMPARATOR AND ZERO CURRENT COMPARATOR						
V_{LLHYS}	Skip hysteresis comparator hysteresis(1)		1	2	3	mV
V_{LLOFF}	Lload hysteresis comparator offset(1)			0	1	mV
V_{ZOFF}	Zero current comparator offset(1)			10	18	mV
T_{HLTOLL}	PWM skip delay time			8		clks
T_{HLTOHL}	Skip to PWM delay time			1		clks
CONTROL LOOP ERROR AMPLIFIER						
I_{EASRC}	COMPx source current		0.2	0.9		mA
I_{EASNK}	COMPx sink current		0.2	0.7		mA
F_{UGB}	Unity gain bandwidth(1)			2.5		MHz
A_{OL}	Open loop gain(1)			80		dB
CMR_{COMP}	COMPx voltage range(1)(6)		0.4		VREG5-3	V
$I_{INVLEAK}$	INVx input current				|0.5|	µA
CONTROL LOOP: DUTY CYCLE, VOLTAGE RAMP, CHANNEL PHASE AND PWM DELAY PATH						
DC_{MAX}	Maximum duty cycle	f_{OSC} = 270 kHz(3)	86%	88%		
		f_{OSC} = 360 kHz	84%	85%		
		f_{OSC} = 450 kHz(2)	80%	82%		
PH_{CH}	Channel to channel phase difference(5)	PWM phase reversal only		180		°
T_{MIN}	OUTX_U minimum pulse width(1)			100		ns
TIMERS: INTERNAL OSCILLATOR(4)						
$f_{OSC(hi)}$	Fast oscillator frequency initial accuracy(2)	R_{SSTRTx} = OPEN		450		kHz
$f_{OSC(lo)}$	Slow oscillator frequency initial accuracy	R_{SSTRTx} = 1MΩ or V_{SSTRT} = 3 V		270		kHz
$f_{OSC(tc)}$	Oscillator frequency over line and temperature	Trimmed for 360 kHz	306	360	414	kHz

(1) Ensured by design. Not production tested.
(2) Maximum 450-kHz frequency can be achieved when both channels are enabled.
(3) 270 kHz is the default frequency during start-up for both channels.
(4) See Table 1.
(5) See PWM detailed description

ELECTRICAL CHARACTERISTICS (continued)

T_A = −40°C to 85°C, 4.5 V < V_{IN} < 20 V, C_{VIN} = 0.1 µF, C_{VREG5} = 2.2 µF, C_{REF_X} = 0.01 µF, PGOOD = 0.2 V, ENBLx = $\overline{DDR}$ = VIN, INVx = COMPx, RSSTRTx = OPEN, TRIP1 = TRIP2 = VIN, LLx = GND, VBSTx = LLX+5, $C_{(OUTx\_U,\ OUTx\_D)}$=1 nF, REG5_IN = 0V, GND = OUTGNDx = 0 V, VO1_VDDQ = VO2 = 0 V (unless otherwise stated)

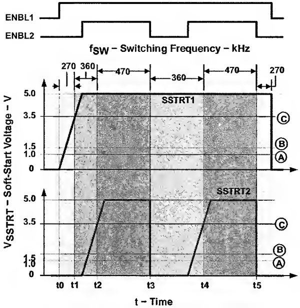
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMERS: SOFT-START RAMP GENERATOR						
I_{SSQ}	SSTRTx charge current	V_{SSTRTx} = 1 V	1.9	2.4	2.8	µA
I_{SSDQ}	SSTRTx discharge current	V_{SSTRTx} = 0.5 V	0.1			mA
V_{REFTRK}	SSTRTx at SMPS regulation point voltage(7)		1.00	1.22	1.45	V
V_{SSOK}	SSTRTx OK to restart voltage		0.23	0.29	0.35	V
V_{SSFIN}	SSTRTx finished voltage(8)		1.4	1.5	1.6	V
V_{SSCLP}	SSTRTx frequency select voltage(9)		3.35	3.50	3.65	V
OUTPUTS: INTERNAL BST DIODE						
V_{FBST}	Forward voltage	(V_{VREF5} − V_{VBSTx})V_{VREF5} = 5 V, I_F = 10 mA T_A = 25°C		0.80	0.85	V
I_{RBST}	Reverse current	V_{RBST}= 30 V		0.1	0.5	µA
OUTPUTS: N-CHANNEL MOSFET GATE DRIVERS						
R_{USRC}	OUTx_U source impedance			3	10	Ω
R_{DSRC}	OUTx_D source impedance			3	10	Ω
R_{USNK}	OUTx_U sink impedance			2.5	5.0	Ω
R_{DSNK}	OUTx_D sink impedance			2.5	5.0	Ω
T_{DEAD}	Gate non-overlap dead time			100		ns

(1) Ensured by design. Not production tested.
(2) Maximum 450-kHz frequency can be achieved only when both channels are enabled.
(3) 270 kHz is the default frequency during start-up for both channels.
(4) See Table 1.
(5) See PWM detailed description
(6) Feedforward Gain can be approximated as follows:
V_{RAMP}= K1×V_{IN}+B1, V_{OFFSET}=K2×V_{IN}x+B2 where K1=0.017, K2=0.01, B1=0.35 V, B2=0.4 V.
At the running duty cycle, the V_{COMP} should be approximately: $V_{COMP} = V_{OUT} \times \left(K1 + \frac{B1}{VIN}\right) + (K2 \times VIN + B2)$
(7) See waveform point A in Figure 1
(8) See waveform point B in Figure 1
(9) See waveform point C in Figure 1

Table 1. Frequency Selection

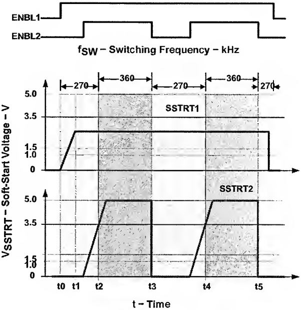
SSTRT1	SSTRT2	FREQUENCY (kHz)
C_{SSTRT} only	C_{SSTRT} only	450(10)
1 MΩ ‖ C_{SSTRT} to GND	C_{SSTRT} only	360
C_{SSTRT} only	1 MΩ ‖ C_{SSTRT} to GND	360
1 MΩ ‖ C_{SSTRT} to GND	1 MΩ ‖ C_{SSTRT} to GND	270

(10)Although selection is made by placing a 1M resistor in parallel with the SSTRTx timing capacitor, the softstart time to 0.85V is altered by about only 20%.



R_{SSTRT1} = R_{SSTRT2} = OPEN = 450 kHz

Figure 1



R_{SSTRT1} = 1 MΩ, R_{SSTRT2} = OPEN = 360 kHz

Figure 2

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
COMP1	2	O	Error amplifier output. Connect feedback network to this pin and INVx for compensation of control loop.
COMP2	14	O	
$\overline{DDR}$	6	I	$\overline{DDR}$ selection pin. If this pin is grounded, the device runs in DDR Mode. The error amplifier reference for VO2 is (VO1_VDDQ)/2, the REF_X output voltage becomes (VO1_VDDQ)/2 and skip mode is disabled for VO2, Also, VREG5 is turned off when both ENBLx are at low in this mode. If this pin is at 2.2-V or higher, the device runs in ordinary dual SMPS mode (dual mode), then the error amplifier reference for VO2 is connected to internal 0.85-V reference, the REF_X output voltage becomes 10 V, VREG5 is kept on regardless of ENBLx status. **CAUTION: Do not toggle $\overline{DDR}$ while ENBL1 or ENBL2 are high.** (See Table 2)
ENBL1	9	I	TTL Enable Input. If ENBLx is greater than 2.2 V, then the VREG5 is enabled (DDR mode) and the SMPS of that channel attempts to turn on. If both ENBL1 and ENBL2 are low then the 10-V (or (VO1_VDDQ)/2 output) voltage as well as the oscillator are turned off. (See Table 2)
ENBL2	10	I	
GND	7	O	Signal ground pin.
INV1	1	I	Error amplifier inverting input. Also input for skip comparator, and OVP/UVP comparators.
INV2	15	I	
LL1	28	I/O	Switch-node connection for high-side driver and overcurrent protection circuitry.
LL2	18	I/O	
OUT1_D	27	O	Synchronous N-channel MOSFET driver output.
OUT2_D	19	O	
OUT1_U	29	O	High-side N-channel MOSFET driver output.
OUT2_U	17	O	
OUTGND1	26	O	Ground return for OUTx_D.
OUTGND2	20	O	

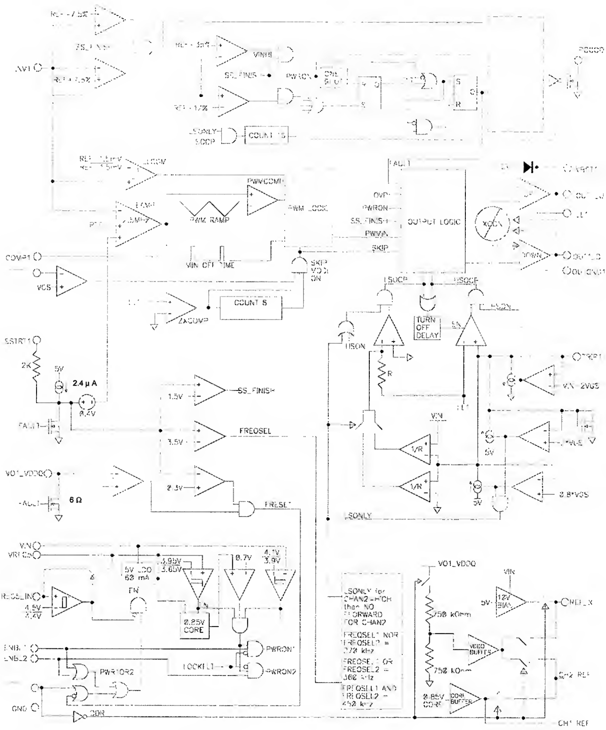
TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
PGOOD	12	O	Power good output. This is an open drain pull-down pin for power good. It remains low during soft-start until both outputs become within ±7.5%. If INV1 or INV2 is out of regulation, or VREG5V goes under UVLO then this pin goes low. The internal delay timer counts 2048 clks at low to high (by design, no delay for high to low). If ENBLx is low, and the power good output is high, then the power good signal for that channel is ignored.
REF_X	8	O	10-V N-channel MOSFET bias or (VO1_VDDQ)/2 reference output. If dual mode is selected ($\overline{DDR}$ > 2.2 V) then this pin provides a low 10-V current (< 2 mA) bias, dropped down from V_{IN}, for the SO – S5 switched N-channel MOSFETs. If DDR mode is selected ($\overline{DDR}$ = GND) then this pin becomes (VO1_VDDQ)/2 capable of 3 mA source current. This bias/reference is shut off when ENBL1 and ENBL2 are both low. (See Table 2)
REG5_IN	21	I	External 5V regulator Input. If this pin is above 4.7 V, then the 5 V circuit bias switches from the VREF5 to the supply presented to REG5_IN.
SSTRT1	3	I	Soft-start/frequency select input. Connect a capacitor between SSTRTx and ground for adjusting the softstart time. A constant current fed to this capacitor ramps the reference during startup. Frequency selection is described in Table 1. The soft-start capacitor is discharged upon UVLO/OVP/UVP, or when ENBLx is asserted low.
SSTRT2	13	I	
$\overline{SKIP}$	4	I	Skip mode selection pin. Ground for automatic control between PWM mode in heavy load and hysteretic operation in light load. Tie high for PWM only operation for the entire load condition. If $\overline{DDR}$ is grounded, then skip mode is disabled for Channel 2.
TRIP1	25	I	Channel 1 overcurrent trip point voltage input. Connect a resistor between TRIP1 and the high-side N-channel MOSFET input conversion voltage for high-side N-channel MOSFET UVP current limit shut down. Connect resistor between TRIP1 and GND for low-side N-channel MOSFET overcurrent latch shutdown.
TRIP2	23	I	Channel 2 overcurrent trip point voltage input. Connect a resistor between TRIP2 and the high-side N-channel MOSFET input conversion voltage for high-side N-channel MOSFET UVP current limit shut down with a 180° channel phase shift. Connect resistor between TRIP2 and GND for low-side N-channel MOSFET over current latch shut-down. The oscillator voltage ramp adjustment (the feed-forward feature) for channel 2 is disabled when this pin is tied to ground via a resistor.
VBST1	30	I	Supply Input for high-side N-channel FET driver. Typically connected via charge pump from LLx.
VBST2	16	I	
VO1_VDDQ	5	I	Output discharge pin. Connect this pin to the SMPS output when discharge is required for power down. The output is discharged to at least 0.3 V before the channel can start-up again. Ground this pin when discharge is not required. When grounded, corresponding channel disables the low side N-channel MOSFET during start-up until the high side N-channel FET attempts to turn on. If $\overline{DDR}$ is low, then the VO1_VDDQ pin must be connected to the VDDQ output since this pin works as the VDDQ feedback to generate the VTT reference voltage and VO2 should be connected to GND since V_{TT} must remain in a high-impedance state during S3 mode.
VO2	11	I	
VREG5	22	O	Internal, 60-mA, 5-V regulator output. $\overline{DDR}$, ENBL1 or ENBL2 high (> 2.2V) turns on the 5 V regulator.
VIN	24	I	High-voltage input. Typically the battery voltage. This pin serves as inputs for the VREF5 regulator, the REF_X regulator and positive input for overcurrent comparators. Precaution should be taken for tracing between this pin and the high-side N-channel MOSFET drain where positive node of TRIPx resistors are located.

Table 2. Reference Regulator Control

MODE	$\overline{DDR}$	ENBL1	ENBL2	VREF5	REF_X	OSC
DDR	LOW	LOW	LOW	OFF	OFF	OFF
DDR	LOW	LOW	HIGH	ON	OFF	ON
DDR	LOW	HIGH	LOW	ON	$\frac{VO1\_DDR}{2}$	ON
DDR	LOW	HIGH	HIGH	ON	$\frac{VO1\_DDR}{2}$	ON
DUAL	HIGH	LOW	LOW	ON	OFF	OFF
DUAL	HIGH	LOW	HIGH	ON	10 V	ON
DUAL	HIGH	HIGH	LOW	ON	10 V	ON
DUAL	HIGH	HIGH	HIGH	ON	10 V	ON

FUNCTIONAL BLOCK DIAGRAM



Shows Channel 1 (VO1_VDDQ) and the supporting circuitry.

APPLICATION INFORMATION

PWM OPERATION

The PWM control block utilizes a fixed-frequency, feed-forward, voltage-mode control scheme with a wide-bandwidth, low-impedance output error amplifier as the voltage servo control block. This scheme allows the highest efficiency down conversion while maintaining excellent line regulation and fast transient response. Loop compensation is programmed by connecting a filter network between the COMPx pin and the INVx pin. The wide bandwidth error amplifier handles conventional Type II compensation or Type III compensation when using ceramic capacitors for the converter output. For channel one, the reference signal for the control loop is always a precision 0.85-V internal reference, while the channel two loop reference is either the 0.85-V reference or, in the case of $\overline{DDR}$ mode, one half the VO1_VDDQ voltage, (VO1_VDDQ)/2. The output signal of the error amplifier appears at the COMPx pin and is compared to a buffered version of the 0.6-V oscillator ramp. When TRIP2 pin is tied to VIN through a resistor, the voltage ramp is further modulated by the input voltage, VIN, to maintain a constant modulator gain. If the TRIP2 pin is connected to ground through a resistor, then the voltage ramp remains fixed regardless of VIN value.

The oscillator frequency is internally fixed and can be selected at 270 kHz, 360 kHz or 470 kHz by insertion of a clamping resistor on the SSTRTx pin per Table 1. For example, 470 kHz can be attained when both SSTRTx voltages exceed 3.5 V, as described in WAVEFORM1. The controller begins with 270 kHz in the first stage of the softstart, and then increases to 470 kHz at the steady state. When 270 kHz is selected, both of SSTRTx voltages are kept below 3.5 V so that the frequency is the same 270 kHz for the entire operation.

Two channels are operated in 180 degrees out-of-phase interleave switching mode. This interleaving helps reduce the input current ripple requirement for the input capacitor. However, because the PWM loop determines both the turn-off AND turn-on of the high-side MOSFET, this 180 degree operation may not be apparent by looking at the LLx nodes only. Rather, the turn-off cycle of one channel always corresponds to the turn-on cycle of the other channel and vise-versa. As a result, input ripple is reduced and dynamic response is improved over a broad input voltage range.

MAXIMUM DUTY CYCLE

Because most notebook applications typically run from three to four cell Li–Ion or run from a 20-V adapter, 100% duty cycle operation is not required. Rather, the TPS51020 is optimized for low duty ratio step-down conversion. As a result of limiting the duty cycle, the flying BST capacitor is refreshed reliably and the low-side over current detection circuitry is capable of detecting an overcurrent condition even if the output is stuck between the regulation point and UVP. The maximum duty cycle for each operating frequency is 88% for 270 kHz, 85% for 360 kHz and 82% for 470 kHz.

It should be noted that if the system is operating close to maximum (or minimum) duty cycle, it may be difficult for the converter to respond quickly during line/load transients or state changes (such as frequency switching during soft start or PWM to SKIP mode transitions). This slow response is due to the dynamic range of the COMP pin and is usually not a result of poor phase compensation. In the case of minimum duty cycle operation, the slow response is due to the minimum pulse width of the converter (100 ns TYP). In this case (counter intuitively), it may be advisable to slow down the switching frequency of the converter in order to improve response time.

APPLICATION INFORMATION

SKIP MODE OPERATION

If the $\overline{\text{SKIP}}$ pin is set HIGH, the SMPS operates in the fixed PWM mode. While a LOW signal is applied, the controller operates in autoskip mode. In the autoskip mode, the operation changes from constant frequency PWM mode to an energy-saving skip mode automatically by detecting the edge of discontinuous current mode. During the skip mode, the hysteretic comparator monitors output voltage to trigger high side on at the next coming oscillator pulse after the lower level is detected. Several sequential pulses may be seen, especially in the intermediate load level, before output capacitor is charged up to the higher level and waits for next cycle. In the skip mode, frequency varies with load current and input voltage.

Skip mode for SMPS_2 is disabled regardless of the $\overline{\text{SKIP}}$ pin status if DDR mode is selected (see *Dual Mode and DDR Mode* section). This is because current sink capability is required for V_{TT}, so that rectifying MOSFET needs to be kept on when the inductor current flows inversely. SMPS_1 is still capable of skip mode operation while DDR Mode.

CASCADE CONFIGURATION

If the TRIP2 pin is tied through a resistor to the input voltage, the TPS51020 assumes that the conversion voltage for channel two is the VIN voltage, usually VBATT. Conversely, if TRIP2 is tied through a resistor to ground, the controller assumes that the conversion voltage for channel two is the output voltage of channel one or some other stable bus voltage.

DUAL MODE AND DDR MODE

TPS51020 provides one-chip solution for system power supply, such as for 5 V, 3.3 V or 1.8 V, and a dual switcher DDR power supply. By simply selecting $\overline{\text{DDR}}$ signal and some external configuration change following the instructions below, TPS51020 gives a complete function set required for the DDR termination supply such as VDDQ/2 tracking V_{TT} source/sink capability and V_{TT} reference output. power

If $\overline{\text{DDR}}$ is set high (> 2.2 V), the TPS51020 runs in dual mode, that is, each converter produces an independent output voltage with respect to the internal 0.85-V reference. Bypass REF_X to ground by 0.01-µF. The VO1_VDDQ or VO2 terminal can be connected to either to their corresponding switcher output or ground, depending on customer's choice of using or not using the output discharge function (See *Softstop*). The 10-V reference output can be used as FET switch biasing for power control during sleep states (see Figure 5). During this dual mode, selection of autoskip mode or PWM mode made by $\overline{\text{SKIP}}$ applies to both SMPS_1 and SMPS_2.

If $\overline{\text{DDR}}$ is set low (< 0.3V), the TPS51020 operates as a dual switcher DDR supply; VDDQ from SMPS_1 and V_{TT} from SMPS_2 (DDR Mode). In this mode, the reference voltage for SMPS_2 is switched to (VO1_VDDQ)/2 to track exactly half the voltage of SMPS_1, divided by internal resistors. VO1_VDDQ should be connected to SMPS_1 output terminal to accomplish this, while VO2 connection is still flexible to the customer's choice of softstop. REF_X outputs the (VO1_VDDQ)/2 voltage after a buffer (5-mA max). $\overline{\text{SKIP}}$ controls only SMPS_1 and SMPS_2 is forced to operate in PWM mode so that current can be sink from the output. Power source of SMPS_2 can either be the battery voltage (independent configuration), or the VDDQ (cascade configuration) by user's preference. When using the independent configuration, TRIP2 needs to be connected to the VIN node via trip resistor. In case of cascade configuration, tie TRIP2 to GND via trip resistor (see Figure 7).

CAUTION:Do NOT toggle $\overline{\text{DDR}}$ HIGH while ENBL1 or ENBL2 is high (see Table 2). REF_X output switches to high voltage (10 V) and be applied to V_{TTREF} directly

APPLICATION INFORMATION

5-V LINEAR REGULATOR (VREG5)

The VREG5 voltage is the bias for all the low voltage circuitry in the TPS51020 as well as the DC boost voltage for the MOSFET gate drivers. Total available current is 60 mA. Bypass this pin to GND by 4.7-µF. The under voltage lockout (UVLO) circuit monitors the output of this regulator to protect internal circuitry from low input voltages. If 5 V is applied to REG5_IN from either the SMPS output or an alternate 5 V, then the linear regulator is turned off and the VREG5 pin is switched over to REG_IN. This operation enhances the efficiency of the overall power supply system because the bulk of the quiescent current now runs from the 5-V output instead of VIN (VBAT). In this configuration, ensure that VREG5_IN is less than or equal to V_{VIN}.

EXTERNAL 5V INPUT (REG5_IN)

When a 5-V bus is available, VIN does not need to be connected to the battery. In this configuration, VIN should be connected to REG5_IN.

LOW-SIDE N-CHANNEL FET DRIVER

The low-side driver is designed to drive high current low $R_{DS(on)}$ N-channel MOSFET(s). The maximum drive voltage is 5.5 V. The drive capability is represented by its internal resistance, which are 3 Ω for VREG5 to OUTx_D and 2.5 Ω for OUTx_D to OUTGNDx. A dead time is internally generated between top MOSFET off to bottom MOSFET on, and bottom MOSFET off to top MOSFET on, in order to prevent shoot through.

The low-side driver is typically turned off during all fault modes except for OVP. When an OVP condition exists, the low-side driver of the offending channel turns on and attempts to blow the protection fuse of the input supply. During power up the low-side driver is kept off until the high side driver attempt to turn on once. In this fashion, the TPS51020 can power up into a precharged output voltage, if so desired.

HIGH-SIDE N-CHANNEL FET DRIVER

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFET(s). When configured as a floating driver, a 5-V bias voltage is delivered from VREG5 supply. The instantaneous drive current is supplied by the flying capacitor between VBSTx and LLx pins, 0.1-µF ceramic for typical applications. The boost diodes are integrated and are sufficient for enhancing the high-side MOSFET. However, external boost diodes can also be added from VREG5 to each VBSTx in case higher gate-to-source votlage is required.

The drive capability is represented by its internal resistance, which are as follows: 3 Ω for VBST to OUTx_U and 2.5 Ω for OUTx_U to LLx. The maximum voltage that can be applied between OUTx_U pin and OUTGNDx pin is 35 V.

APPLICATION INFORMATION

ENABLE AND SOFT-START

Each SMPS is switched into standby mode separately by grounding the corresponding ENBLx pin. The 5-V supply is enabled if either the $\overline{\text{DDR}}$, ENBL1 or ENBL2 pin(s) goes high (>2.2 V).

Softstart of each SMPS is achieved by slowly ramping the error amplifier reference voltage by following a buffered version of the SSTRTx pin voltage. Designers can achieve their own start-up sequencing by simply provide external timing signals since the startup times do not depend on the load current. The softstart time is programmable by external capacitor connected from SSTRTx pin to the ground. Each SSTRTx pin sources constant current, typically 2.3 µA. The output voltage of the SMPS ramps up from 0 V to its target regulation voltage as the SSTRTx pin voltage increases from 0 V to 1 V. This gives the softstart time formula to be,

$$C_{SSTRT}\,(\text{Farads}) = T_{SSTRT}\,(\text{sec}) \times 2.3 \times 10^{-6}$$

The soft-start capacitor is discharged upon UVLO, OVP or UVP is detected as well as ENBLx is set low.

OUTPUT DISCHARGE (SOFT-STOP)

When an SMPS is turned off by ENBLx asserted low or the part enters a fault mode, both top and bottom drivers are turned off. This may leave the output in a high impedance state that allows the voltage to persist for some time. If this voltage is undesirable, then user can connect the output to the VO1_VDDQ or VO2 pins.

These pins turn on a 6-Ω resistor to ground during an off or fault condition. Both the VO1_VDDQ and VO2 pin must be discharged to 0.3 V before the TPS51020 restarts. Grounding VO1_VDDQ or VO2 inhibits output discharge for each SMPS, respectively. The TPS51020 has the flexibility of adding a resistor in series with the VOx pin and the output voltage in order to reduce the discharge current and reduce the total power dissipation within the device. It should be noted that when this resistor is added the discharged voltage threshold changes according to the following equation:

$$V_{DISCHARGE} = \frac{\left(R_{EXTERNAL} + R_{DS(on)}\right)}{R_{DS(on)}} \times 0.3$$

where

- $R_{EXTERNAL}$ is the series resistor between VOx and the output
- $R_{DS(on)} = 6\ \Omega$

When grounded, corresponding channel disables the low-side MOSFET during softstart until the high-side MOSFET attempts to turn on. This allows the user to start up with precharged output.

APPLICATION INFORMATION

10-V N-CHANNEL FET BIAS or (VOUT1)/2 VTT VOLTAGE REFERENCE (REF_X)

TPS51020's REF_X provides two functions depending on the operational mode. One is a linear regulator that supply 10-V for FET switch biasing in the dual mode, the other is V_{TT} reference voltage in the DDR mode.

If $\overline{DDR}$ is high (> 2.2 V) then the REF_X output is a convenient 10-V, 2-mA (maximum) output, useful for biasing N-channel FET switches typically used to manage S0, S3 and S5 sleep states where the main supply is switched to many outputs. When V_{IN} is < 12 V, REF_X approximately tracks V_{IN}−2 V.

If $\overline{DDR}$ is low, then the REF_X output becomes the VDDQ/2 (VO1_VDDQ/2) reference. This output is capable of 5-mA source current and is left on even if channel two (V_{TT} switcher) is turned off. REF_X is turned off if ENBL1 and ENBL2 are both low (see Table 2).

POWERGOOD

The TPS51020 has advanced powergood logic that allows single powergood circuit to monitor both SMPS output voltages (see Figure 3).

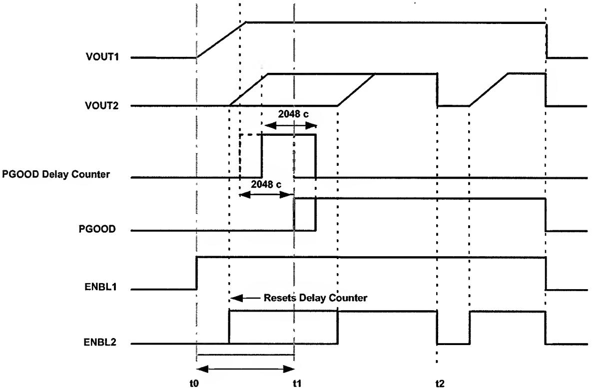


Figure 3. PowerGood Timing Diagram

The PGOOD terminal is an open drain output. The PGOOD pin remains low until both power supplies have started and have been in regulation (±7.5%) for 2048 clock pulses.

APPLICATION INFORMATION

If one channel is enabled in the period between T0 and T1, (the other channel's ramp time plus delay time,) the PGOOD delay counter restarts counting softstart finish after the last channel has finished softstart. Enabling after T1 is ignored by PGOOD until the channel finishes its softstart. If either of the SMPS output goes out by ± 7.5% or UVLO is detected while ENBLx is high, PGOOD pulls low. If a channel is disabled while the other is still active PGOOD maintains it's logic state and only monitor the active channel.

PROTECTION FUNCTIONS

The TPS51020 is equipped with input undervoltage lock out (UVLO), output undervoltage protection (UVP) and overvoltage (OVP) protection. Overcurrent is detected using $R_{DS(on)}$ of the external power MOSFETs and protected by triggering UVP, or latch off in some cases. The states of output drive signal depends on which protection was involved. Please refer to each protection description below for the detail.

When the input voltage UVLO is tripped, the TPS51020 resets and waits for the voltage to rise up over the threshold voltage and restart the device. Alternatively, if output UVP or OVP is triggered, the device latches off after a delay time defined by the internal fault counter counting the PWM oscillator pulses. The VREF5 and REF_X is kept on in this latch off condition. The fault latch can be reset by toggling both of ENBLx pins in DDR mode. The fault latch can be reset by either toggling VIN or bringing $\overline{\text{DDR}}$, ENBL1 and ENBL2 all low. Be sure to bring $\overline{\text{DDR}}$ high prior to ENBLx when TPS51020 is being used in dual mode.

If a false trip of the UVLO appears due to input voltage sag during turn-on of the high-side MOSFET such as a large load transient, first consider adding several micro-farads of input capacitance close to the MOSFET's drain. Also consider adding a small V_{IN} filter, ex. a 2.2-Ω resistor and a 2.2-µF, for decoupling. The trip resistors should be connected to the same node as VIN pin of the device when this filter is applied. The filter resistor should be as small as possible since a voltage drop across this resistor biases the OCP trip point.

UNDERVOLTAGE LOCKOUT PROTECTION

There are two undervoltage lock out protections (UVLO) in TPS51020. One is for V_{IN}, which has a typical trip threshold voltage 3.9 V and trip hysteresis 200 mV. The other is for VREF5, which has a typical trip threshold voltage 3.65 V and trip hysteresis 300 mV. If either is triggered, the device resets and waits for the voltage to rise up over the threshold voltage and restart the part. Please note this protection function DOES NOT trigger the fault counter to latch off the part.

OVERVOLTAGE PROTECTION

For overvoltage protection (OVP), the TPS51020 monitors INVx voltage. When the INVx voltage is higher than 0.95V (+12%), the OVP comparator output goes high (after a 20-µs delay) and the circuit latches the top MOSFET driver OFF, and bottom driver ON for the SMPS detected overvoltage. In addition, the output discharge (softstop) function is enabled to discharge the output capacitor if VO1_DDR, VO2 is connected to corresponding output terminal. The fault latch can be reset by either toggling VIN or bringing $\overline{\text{DDR}}$, ENBL1 and ENBL2 all low. Be sure to bring $\overline{\text{DDR}}$ high prior to ENBLx when TPS51020 is being used in dual mode.

UNDERVOLTAGE PROTECTION

For undervoltage protection (UVP), the TPS51020 monitors INVx voltage. When the INVx voltage is lower than 0.55 V (–35 %), the UVP comparator output goes high, and the internal FLT timer starts to count PWM oscillator pulses. After 4096 clock pulses, the part latches off. Both top and bottom drivers are turned off at this condition. Output discharge (soft-stop) function is enabled to discharge the output capacitor if VO1_DDR, VO2 is connected to corresponding output terminal. The fault latch can be reset by either toggling VIN or bringing $\overline{\text{DDR}}$, ENBL1 and ENBL2 all low. Be sure to bring $\overline{\text{DDR}}$ high prior to ENBLx when TPS51020 is being used in dual mode.

APPLICATION INFORMATION

OVERCURRENT PROTECTION

Overcurrent protection (OCP) is achieved by comparing the drain to source voltage of the high-side and low-side MOSFET to a set point voltage. This voltage appears at the TRIPx pin and is defined by the conversion voltage, typically VIN, minus the I × R drop of the I_{TRIP} current flowing through the external resistor connected to the conversion voltage. The offset of the internal comparators also plays a role in determining the overall accuracy and set point of the OCP limit.

When the drain-to-source voltage of the synchronous MOSFET exceeds the set point voltage created by the I × R drop (usually 20 mV to around 150 mV), the synchronous MOSFET on-time is extended into the next pulse and the high-side MOSFET OCP comparator is enabled. If during the subsequent high-side on-time the drain-to-source voltage of the high-side MOSFET exceeds the set point voltage, then the high-side on-time pulse is terminated. This low-side extension/high-side termination action has the effect of decreasing the output voltage until the UVP circuit is activated to turn off both the high-side and low-side drivers. The TPS51020 I_{TRIP} current has a temperature coefficient of 4200 PPM/°C.

The threshold voltage for the OCP comparator is set by I × R drop across the trip resistor. The I_{TRIP} current is 12.5-μA (typ) at R.T. so that the OCP point is given by following formula,

$$R_{TRIP} = \frac{R_{DS(on)} \times \left(I_{OCP} - \frac{I_{RIPPLE}}{2}\right)}{12.5 \times 10^{-6}}$$

Precaution should be taken with board layout in order to design OCP point as desired. The conversion voltage point must avoid high current path. Any voltage difference between the conversion point and VIN input for the TPS51020 is included in the threshold voltage. VIN plane layout should consider the other channels high-current path as well.

A brief discussion is required for TRIP2 function. When TRIP2 is connected, via a resistor to GND, only low-side OCP is used. This is the case for cascade configuration been selected. In this mode, UVP does not play a roll in the shut off action and there is only a short delay between the over current trigger level been hit and the power MOSFETs turn off. However, as with UVP, the SSTRTx pins are discharged and both SMPS goes though a restart.

LAYOUT CONSIDERATIONS

Below are some points to consider before the layout of the TPS51020 design begins.

- Signal GND and power GND should be isolated as much as possible, with a single point connection between them.
- All sensitive analog components such as INV, SSTRT, SKIP, $\overline{\text{DDR}}$, GND, REF_X, ENBL and PGOOD should be reference to signal GND and be as short as possible.
- The source of low-side MOSFET, the Schottky diode anode, the output capacitor and OUTGND should be referenced to power GND and be as short and wide as possible, otherwise signal GND is subject to the noise of the outputs.
- PCB trace defined as the node of LL should be as short and wide as possible.
- Connections from the drivers to the gate of the power MOSFET should be as short and wide as possible to reduce stray inductance and the noise at the LL node.
- The drain of high-side MOSFET, the input capacitor and the trip resistor should be as short and wide as possible. For noise reduction, a 22-pF capacitor C_{TRIP} can be placed in parallel with the trip resistor.

APPLICATION INFORMATION

- The output voltage sensing trace and the feedback components should be as short as possible and be isolated from the power components and traces.
- The low pass filter for VIN should be placed close to the TPS51020 and be referenced to signal GND.
- The bootstrap capacitor C_{BST} (connected from VBST to LL) should be placed close to the TPS51020.
- VREG5 requires at least 4.7-µF bypass capacitor which should be placed close to the TPS51020 and be referenced to signal GND.
- The discharge (VO1_VDDQ, VO2) should better have a dedicated trace to the output capacitor. In case of limiting the discharge current, series resistors should be added.
- Ideally, all of the area directly under the TPS51020 chip should also be signal GND.

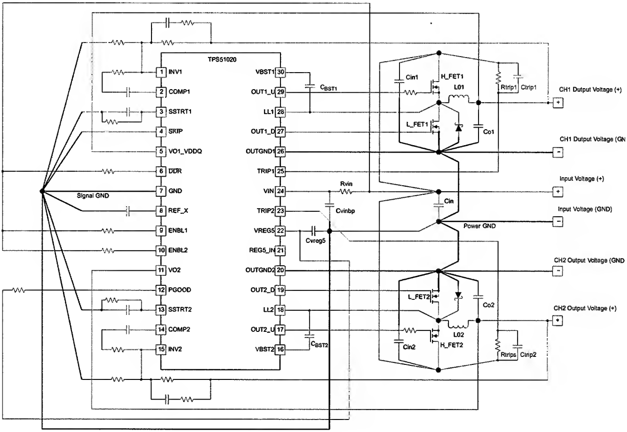


Figure 4. PCB Trace Guideline

APPLICATION INFORMATION

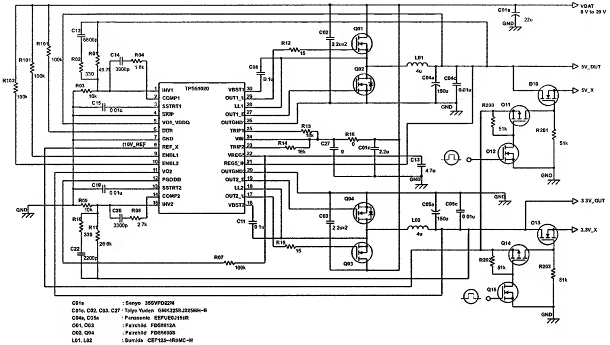


Figure 5. Typical Application Circuit: Dual (5V/6A + 3.3V/6A) from VBAT

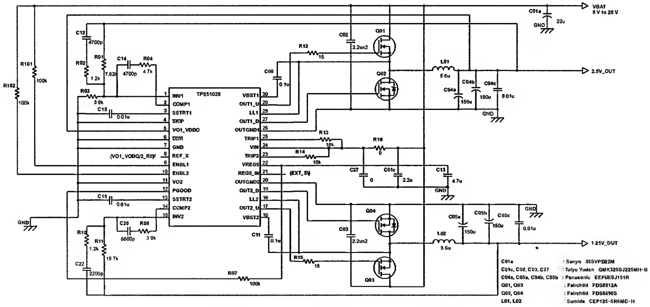
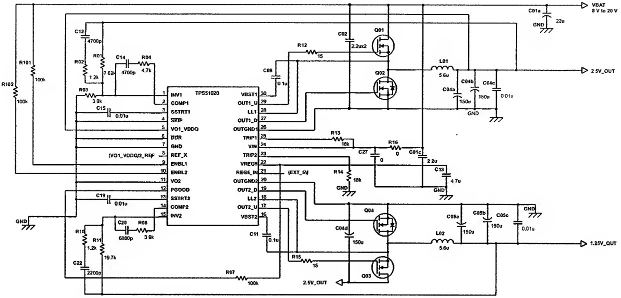


Figure 6. Typical Application Circuit: DDR(2.5V/6A + 1.25V/6A) from VBAT

APPLICATION INFORMATION



C01a	: Sanyo 35SVPD22M
C01c, C02, C27	: Taiyo Yuden GMK325BJ225MH–B
C04a, C05a, C04b, C05b, C04d	: Panasonic EEFUE0J151R
Q01, Q03	: Fairchild FDS6612A
Q02, Q04	: Fairchild FDS6690S
L01, L02	: Sumida CEP125–5R6MC–H

Figure 7. Typical Application Circuit: DDR (2.5V/6A + 1.25V/3A) Cascade

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs JUNCTION TEMPERATURE

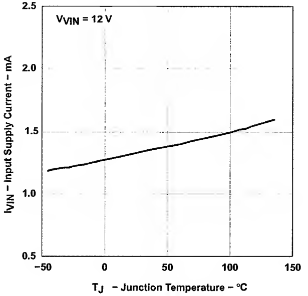


Figure 8

SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

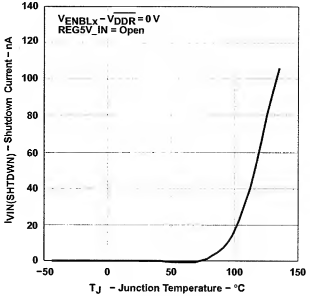


Figure 9

TRIP CURRENT vs JUNCTION TEMPERATURE

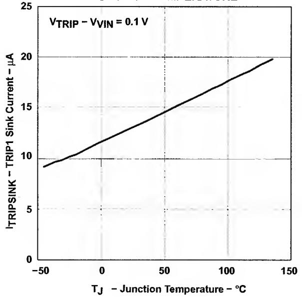


Figure 10

SOFTSTART CURRENT vs JUNCTION TEMPERATURE

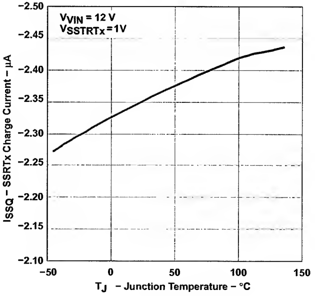


Figure 11

TYPICAL CHARACTERISTICS

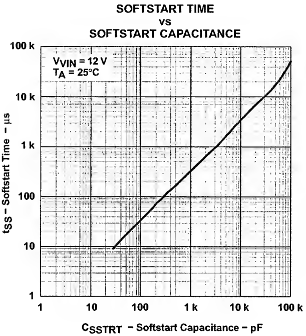


Figure 12

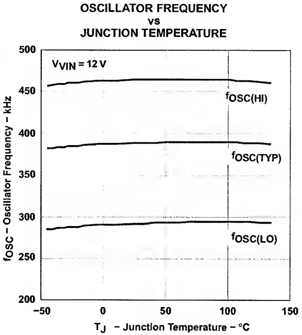


Figure 13

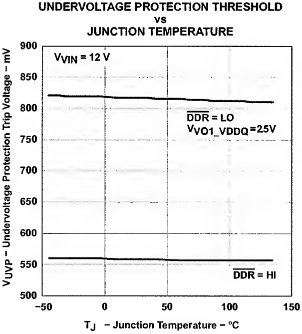


Figure 14

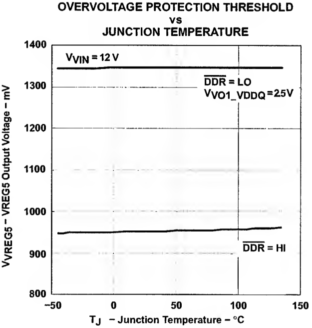


Figure 15

TYPICAL CHARACTERISTICS

VREG5 OUTPUT VOLTAGE
vs
VREG5 OUTPUT CURRENT

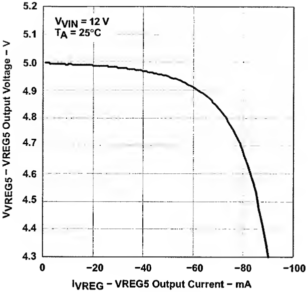


Figure 16

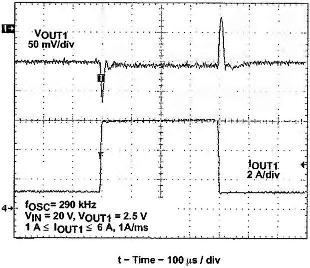


Figure 17. Load Transient Response

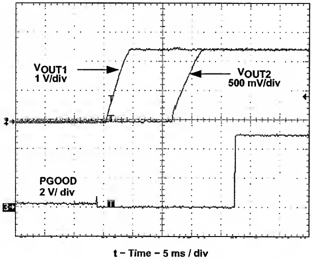


Figure 18. Simultaneous Startup

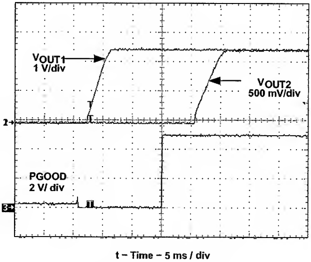


Figure 19. Offset Startup

TYPICAL CHARACTERISTICS

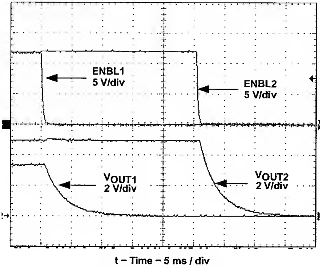


Figure 20. Soft-Stop

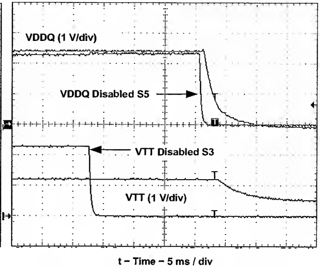


Figure 21. Cascade Configuration DDR Mode Shudown

PWM MODE EFFICIENCY
vs
OUTPUT CURRENT

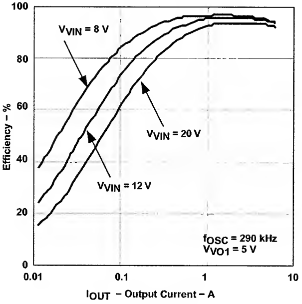


Figure 22

AUTOSKIP MODE EFFICIENCY
vs
OUTPUT CURRENT

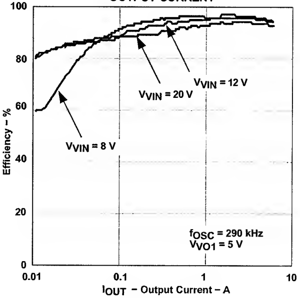


Figure 23

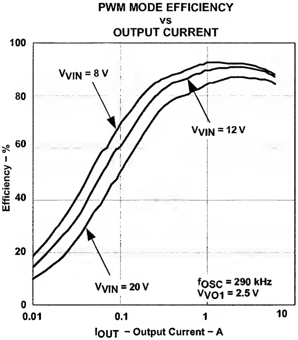


Figure 24

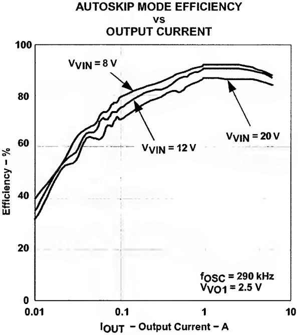
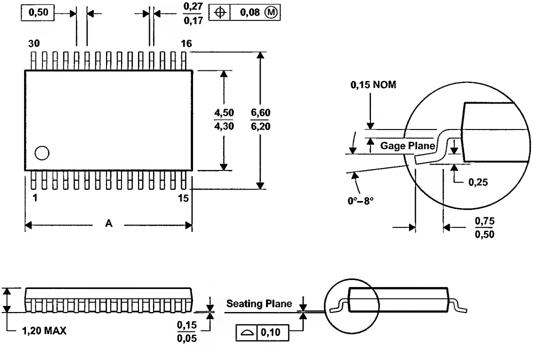


Figure 25

DBT (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

30 PINS SHOWN



PINS ** / DIM	20	24	28	30	38	44	50
A MAX	5,10	6,60	7,90	7,90	9,80	11,10	12,60
A MIN	4.90	6,40	7,70	7,70	9,60	10,90	12,40

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153

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